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NITRIDE OFFSET SPACER TO MINIMIZE SILICON RECESS BY USING POLY REOXIDATION LAYER AS ETCH STOP LAYER

FIELD OF THE INVENTION

[01] The present invention relates to the field of semiconductor device manufacturing, and more particularly, to the use of offset spacers during the formation of a semiconductor device.

BACKGROUND OF THE INVENTION

[02] As the minimum feature size in semiconductor integrated circuits shrinks, the distance between the source and the drain regions becomes smaller. The reduced spacing between the source and drain regions for the field-effect transistors (FETs) results in short channel effects such as punch-through, reduced source-to-drain breakdown voltage, reduced threshold voltage (V_t), and increased sub-threshold swing. To relieve the short channel effects, the semiconductor industry is constantly optimizing the fabrication processes for MOSFET devices. Current trends in VLSI fabrication of CMOS devices are toward reducing the junction depth of the source/drain regions because shallow junctions reduce encroachment of the source/drain depletion regions into the channel.

[03] Advances in semiconductor processing technology have reduced channel lengths to well below 0.25 μm. At these sizes, any loss of effective channel length can be costly in terms of lowering the breakdown voltage of a transistor. Accordingly, limiting the lateral diffusion of the source/drain impurities is increasingly important.

[04] A halo implant, also called a "pocket implant", can limit the lateral diffusion of the source and drain impurities. The halo implants impurities have a conductivity type opposite to that of the source and drain. Usually, the halo implant comes after defining the gate and before the source/drain diffusion. Due to the masking effect, the halo implant typically exhibits peak impurity concentration near the source/drain regions. To impede vertical diffusion of source/drain impurities, the implant energy for the halo implant should be carefully chosen so that the halo depth away from the peak is greater than the depth of the source/drain implant.

[05] In order to reduce the overlap capacitance between the gate electrode and the drain, and thereby provide better AC performance for the transistor, it is desirable to separate the halo and the

extension. Accordingly, offset spacers have been employed that are formed on the sides of a gate electrode. By forming a halo, followed by the formation of an offset spacer on the sidewalls of gate electrode, and then formation of the source/drain extensions, the halo is physically located in front of the extension. Use offset spacers makes the effective channel length longer for a given physical channel length.

[06] In the formation of offset spacers, a dielectric layer is typically deposited over the substrate and a gate electrode. An anisotropic etch is performed to clear the substrate on top of the gate electrode of the dielectric layer while leaving a portion of the dielectric layer on the gate sidewalls. This portion of the dielectric layer remaining on the gate sidewalls forms the offset spacer. Materials that have been described for use as the offset spacers includes silicon oxide and silicon nitride. Once the offset spacer is formed, a source/drain extension implant is performed using the offset spacer as a mask. Continued processing steps include the formation of sidewall spacers over the offset spacers followed by deep source/drain implants.

[07] The formation of the offset spacers in the above-described manner creates a problem in that the anisotropic etching gouges the silicon substrate caused by overetching of the dielectric layer from which the offset spacers are formed. This situation is depicted schematically in Figures 1 and 2. In Figure 1, a substrate 10 has a gate electrode 12 on its surface. A dielectric layer 14 covers the substrate 10 and the gate electrode 12. An anisotropic etching is performed that removes the dielectric material 14 from the substrate to form the offset spacer 16. However, a recess 18 is also formed by the gouging of the substrate 10 caused by the overetching, since it is difficult to stop on silicon in anisotropic etching processes. The formation of the recess 18, especially in the source/drain extension area is a concern. This is because silicon gouging is equivalent to increasing junction depth, which is undesirable as shallow depth junctions are sought after in today's technologies. Also, the overlap capacitance is adversely affected by the gouging created during offset spacer creation.

[08] There is a need for a method of forming a semiconductor device with offset spacers in a manner that prevents gouging of the silicon substrate during the etching of the dielectric layer that forms the offset spacers.

SUMMARY OF THE INVENTION

[09] These and other needs are met by embodiments of the present invention which provide a method of forming a semiconductor device, comprising the steps of forming a gate electrode on substrate and forming a polysilicon reoxidation layer over the substrate and the gate electrode. A

nitride layer is deposited over the polysilicon reoxidation layer. The nitride is anisotropically etched, with this etching stopping on the polysilicon reoxidation layer to form nitride offset spacers on the gate electrode. The use of the polysilicon reoxidation layer as an etch stop layer during the formation of the nitride offset spacers prevents the gouging of the silicon substrate in accordance with embodiments of the present invention. The very thin polysilicon reoxidation layer may be left on the substrate, and implantation may controllably and reliably be made through the remaining polysilicon reoxidation layer to form the source/drain extensions and source/drain regions. Alternatively, the polysilicon reoxidation layer may be removed by a wet etch, without creating the gouging normally associated with dry etching of a dielectric layer.

[10] The earlier cited needs are also met by embodiments of the present invention which provide a method of performing a semiconductor device with halo implants, comprising the steps of forming a gate electrode on a substrate and forming an etch stop layer on the substrate. A nitride layer is formed on the substrate and on the gate electrode. The nitride layer is etched to form offset spacers on the gate electrode, with the etching stopping on the etch stop layer.

[11] The foregoing and other features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[12] Figure 1 is a schematic depiction of a cross-section of a semiconductor device during formation of the device in accordance with the prior art.

[13] Figure 2 shows the structure of Figure 1 following dry etching of a dielectric layer with gouging of the substrate, in accordance with methods of the prior art.

[14] Figure 3 shows a substrate and gate electrode during the formation of a semiconductor device in accordance with embodiments of the present invention.

[15] Figure 4 depicts the structure of Figure 3, following the formation of a polysilicon reoxidation layer over the substrate and the gate electrode, in accordance with embodiments of the present invention.

[16] Figure 5 chose the structure of Figure 4, after a nitride layer has been deposited over the polysilicon reoxidation layer, in accordance with embodiments of the present invention.

[17] Figure 6 depicts the structure of Figure 5, after anisotropic etching has been performed to remove horizontal portions of the nitride layer, in accordance with embodiments of the present invention.

[18] Figure 6A shows an embodiment of the present invention in which a portion of the polysilicon reoxidation layer is removed by a wet etching process, in accordance with certain embodiments of the invention.

[19] Figure 7 depicts the structure of Figure 6, after a source/drain extension has been implanted into the substrate, in accordance with embodiments of the present invention.

[20] Figure 8 shows the structure of Figure 7, after a source/drain implant step has been performed, in accordance with embodiments of the present invention.

[21] Figure 9 depicts a gate electrode formed in accordance with an aspect of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[22] The present invention addresses and solves problems related to the formation of offset spacers in the creation of semiconductor devices. In particular, the present invention solves, in part, the problems of gouging that arises during the etching of a dielectric layer to form the offset spacers on the sidewalls of gate electrodes. The present invention achieves this, in part, by providing an etch stop layer, such as a polysilicon reoxidation layer, on the substrate of the semiconductor device. A nitride layer is deposited over the polysilicon reoxidation layer. The anisotropic etching of the nitride layer is selected so that the etching stops on the polysilicon reoxidation layer, rather than continuing through and gouging the silicon substrate. Since the polysilicon reoxidation layer is very thin, the implantation process may be controllably and reliably performed through the polysilicon reoxidation layer to form source/drain extensions and source/drain regions. Alternatively, the polysilicon reoxidation layer may be safely removed by a wet etch process without fear of gouging a silicon substrate. The prevention of gouging allows the separation of the halo and the extension, and reduces the overlap capacitance to provide better AC performance of the transistor. Also, the present invention, by preventing silicon gouging, maintains the effectiveness of shallow depth formation.

[23] Figure 3 depicts a cross section of a semiconductor device during formation of the device and in accordance with embodiments of the present invention. This device includes a substrate 20 made from silicon, for example. On the top surface of the substrate 20, a gate electrode made of polysilicon, for example, is provided. Formation of the polysilicon gate electrode 22 may be conventional, and

may include formation of a gate oxide followed by deposition of polysilicon or other gate electrode material, and etching to form the gate electrode 22.

[24] Pictured in Figure 3 are halo implants 24. The halo implants 24 are provided in a conventional halo implant process. Although halo implants 24 are depicted throughout the methodology of the present invention, it is to be understood that the halo implants 24 are optional and embodiments of the present invention form semiconductor devices without such halo implants. These embodiments are not depicted in Figures 3 - 8, but one of ordinary skill in the art would understand that the methodology of the present invention may be performed with or without halo implants 24. However, for purposes of illustration and example, the halo implants 24 are shown in Figures 3 - 8.

[25] Figure 4 depicts the structure of Figure 3 following a polysilicon reoxidation step in accordance with embodiments of the method of the present invention. The polysilicon reoxidation step forms a polysilicon reoxidation layer 26 over the surface of the substrate 20 and the gate electrode 22. The polysilicon reoxidation layer 26 is formed by a conventional polysilicon reoxidation formation process, which provides a thermally grown oxidation layer at temperatures between about 750°C to 900°C. The polysilicon reoxidation layer 26 is formed to a thickness of between 15 to about 50 Å, a preferred thickness being about 25 Å. The polysilicon reoxidation layer 26 is a very dense, high quality dielectric layer that will provide better selectivity as an etch stop layer in a subsequent etching step as described below.

[26] In Figure 5, a nitride layer 28 has been deposited conformally over the polysilicon reoxidation layer 26. The nitride layer 28, which may be made of silicon nitride, for example, can be deposited in a conventional manner by plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD), as exemplary techniques. Nitride may be deposited at thicknesses of between about 100 to about 500 Å. An exemplary embodiment of the invention employs a thickness of about 250 Å of deposited nitride.

[27] Following the deposition of the nitride layer 28, an anisotropic etch step is performed, the results of which are shown in Figure 6. The anisotropic etch may be a reactive ion etch, using CHF_3, for example. The etching proceeds to remove the nitride layer 28 from horizontal surfaces, such as the top of the gate electrode 22 and the substrate 20. The polysilicon reoxidation layer 26 serves as an etch stop layer so that etching is stopped on the polysilicon reoxidation layer 26. This prevents the gouging of the silicon substrate 20 during the etching of the nitride layer 28. In prior art methodologies, the etching proceeds into the substrate and would form gouges and recesses, as described earlier, with undesirable consequences. The polysilicon reoxidation layer 26 provides an

excellent selectivity as the nitride/oxide selectivity for an etchant is typically greater than an oxide/silicon selectivity or a nitride/silicon selectivity. Hence, the etching of the nitride layer 28 may be reliably stopped on the polysilicon reoxidation layer 26.

[28] The offset spacers 30 are formed by a nitride portion 32 and a polysilicon reoxidation portion 34 on the sidewall of the gate electrode 22. As shown in Figure 6A, portions of the polysilicon layer 26 that served as an etch stop layer during the anisotropic etching may be removed in certain embodiments by a wet etch process to expose the top surface of the substrate 20. An exemplary wet etch process that will remove the polysilicon reoxidation layer 26 without attacking significantly the silicon substrate 20 is a 100:1 HF solution. The removal of the polysilicon reoxidation layer 26 over the substrate 20 provides an unimpeded path for implantation of the source/drain extensions and the source/drain regions. However, in certain other embodiments of the invention, the polysilicon reoxidation layer 26 over the substrate 20 may be allowed to remain on the substrate 20. This is because the thickness of the polysilicon reoxidation layer 26 on the substrate is so relatively thin that implantations through the polysilicon reoxidation layer 26 into the substrate 20 may be reliably and controllably made. The remainder of the description and the figures will assume the polysilicon reoxidation layer 26 has been allowed to remain on the substrate 20. However, it should be clearly understood that other embodiments of the present invention provide for removal of the polysilicon reoxidation layer 26.

[29] Following formation of the offset spacers 30, as depicted in Figure 7, a source/drain extension implant is performed to create source/drain extensions 36. During this implantation, the offset spacers 30 act as a mask, as is conventionally understood.

[30] In Figure 8, sidewall spacers 38 have been formed which act as masks over the source/drain extensions 36. A source/drain implant is then performed to create source/drain regions 40 in substrate 20. The implants are followed by an activation annealing step in accordance with conventional practices.

[31] The present invention thus provides the benefit of offset spacers, but without the gouging exhibited in prior art semiconductor devices that used offset spacers. This is accomplished by the use of an etch top layer under the dielectric layer from which the offset spacers are etched in an anisotropic etch step.

[32] Another aspect of the invention prevents boron penetration and prevents the undesirable silicidation of the entire polysilicon gate electrode, which can cause gate oxide reliability problems. Also, this aspect produces less polysilicon depletion.

[33] As devices scale down, thin polysilicon is required. However, for thin polysilicon, the boron penetration problem becomes worse. Furthermore, the polysilicon may be too thin so that the entire polysilicon may be silicided, as mentioned above. This makes the poly/ate oxide interface rough and causes the gate oxide reliability problems. As depicted in Figure 9, the invention forms a metal nitride barrier layer 50 over the gate oxide 52 and prior to the depositing of the polysilicon 54, to prevent boron penetration. Also, a later silicidation stops on this conductive metal nitride barrier layer 50. Other benefits of this process include little or no polysilicon depletion.

[34] Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and it is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.